CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

at least one semiconductor chip having at least one lateral power transistor device formed therein; said chip having an upper surface and one or more source, and drain terminals on said upper surface thereof; each of said source and drain terminals having a conductive ball or pillar bump thereon;

a metal lead frame spanning said upper surface of said chip, said metal lead frame being in electrical contact with said conductive balls or pillar bumps; and

a capsule encasing said chip and at least a portion of said metal lead frame.

2. The semiconductor package as in claim 1 wherein said chip further comprises a one or more gate terminals on said upper surface thereof; each of said gate terminals having a conductive ball or pillar bump thereon.

3. The semiconductor package as in claim 1 wherein said opposite ends of said metal lead frame protrudes from opposite sides of said capsule.

4. The semiconductor package as in claim 1 wherein said pillar bumps comprise copper and a conductive solder.

5. The semiconductor package as in claim 1 wherein said balls comprise a conductive solder.

6. The semiconductor package as in claim 1 wherein said lateral power transistor device comprises a lateral power metal oxide field effect transistor.

7. The semiconductor package as in claim 1 wherein said lead frame comprises a conductive metal.

8. The semiconductor package as in claim 2 wherein said conductive metal comprises copper.

9. The semiconductor package as in claim 1 wherein said capsule comprises a non-conductive molding compound.

10. The semiconductor package as in claim 9 wherein said capsule comprises plastic.

11. The semiconductor package as in claims 3 wherein said conductive solder comprises tin.

12. A semiconductor device, comprising:

at least one monolithic semiconductor structure having at least one pair of lateral power transistor device combined on a single semiconductor substrate formed therein; said structure having an upper surface and one or more source and drain terminals on said upper surface thereof; each of said source and drain terminals having a conductive ball or pillar bump thereon;

a metal lead frame spanning said upper surface of said chip, said metal lead frame being in electrical contact with said conductive balls or pillar bumps; and

a capsule encasing said chip and at least a portion of said metal lead frame.

13. The semiconductor package as in claim 12 wherein said structure further comprises one or more gate terminals on said upper surface thereof; each of said gate terminals having a conductive ball or pillar bump thereon.

14. The semiconductor package as in claim 12 wherein said opposite ends of said metal lead frame protrudes from opposite sides of said capsule.

15. The semiconductor package as in claim 12 wherein said pillar bumps comprise copper and a conductive solder.

16. The semiconductor package as in claim 12 wherein said balls comprise a conductive solder.

17. The semiconductor package as in claim 12 wherein said lateral power transistor device comprises a lateral power metal oxide field effect transistor.

18. The semiconductor package as in claim 12 wherein said lead frame comprises a conductive metal.

19. The semiconductor package as in claim 18 wherein said conductive metal comprises copper.

20. The semiconductor package as in claim 12 wherein said capsule comprises a non-conductive molding compound.

21. The semiconductor package as in claim 20 wherein said capsule comprises plastic.

22. The semiconductor package as in claim 12 wherein said lateral power transistor device comprises one or more analog integrated circuit.

23. The semiconductor package as in claim 12 wherein said lateral power transistor device comprises an integrated MOSFET and analog circuit structure.

24. The semiconductor package as in claim 1 wherein said lateral power transistor device comprises one or more analog integrated circuits.

25. The semiconductor package as in claim 1 wherein said lateral power transistor device comprises an integrated MOSFET and analog circuit structure.